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Attorney's Docket No.: 42P8931C Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:
Sujat Jamil et al.

Application No. 10/620,629

Filed: July 15, 2003

For: METHOD AND APPARATUS FOR SCALABLE DISAMBIGUATED CONHERENCE IN SHARED STORAGE HIERARCHIES

Examiner: Verbrugge, K.

Art Unit: 2188

CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office,
Fax No. (703)_872-9306__
on 11-30-04 Lawrence Mennemeier
Date

Assistant Commissioner for Patents
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Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 together with copies of the documents cited on that form. It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

__X__ 37 C.F.R. §1.97(b).

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If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 11-30-04

Lawrence M. Mennemeier
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Substitute for Form 1449A/PTO (Modified)	Attorney Docket No.: 042P8931C	Application Number: 10/620,629
Sheet 1 of 4	First Named Inventor: Sujat Jamil	Examiner Verbrugge, K.
	Filing Date: July 15, 2003	Art Unit: 2188

U.S. PATENT DOCUMENTS

Exam. Initial*	Cite No.[1]	U.S. Patent Document Number	U.S. Patent Document Kind Code[2] (If known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

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	BA	0 397 994 A2		International Business Machines Corporation	11/22/1990	

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Sheet 2 of 4	First Named Inventor: Sujat Jamil	Examiner Verbrugge, K.
	Filing Date: July 15, 2003	Art Unit: 2188

OTHER ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation[2]
	A08	AGARWAL, A., et al., "The MIT Alewife Machine: A Large-Scale Distributed-memory Multiprocessor," *Technical Report MIT/LCS Memo TM-454, Laboratory for Computer Science, Massachusetts Institute of Technology*, 1991.	
	A19	ANDERSON, C., et al., "A Multi-Level Hierarchical Cache Coherence Protocol for Multiprocessors," University of Washington",1992, 92-10-04	
	A18	ANDERSON, C., et al.,. "Design and Evaluation of a Subblock Cache Coherence Protocol for Bus-Based Multiprocessors," University of Washington, 1994, 94-05-02	
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	B01	CENSIER, L.M., et al., "A New Solution to Coherence Problems in Multicache Systems," IEEE Transactions on Computers, Vol. C-27, No. 12, December, 1978, 7 pages	
	A20	CHAIKEN, D., et al., "LimitLESS Directories: A Scalable Cache Coherence Scheme," *Proceedings of the 4th Int'l Conference on ASPLOS*, pages 224-234, New York, April 1991.	
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	A11	FLEISCH, B., "A Coherent Distributed Shared Memory Design," *Proceedings from the 14th ACM Symposium on Operating System Principles*, pages 211-223, New York, 1989.	

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Sheet 3 of 4	First Named Inventor: Sujat Jamil	Examiner Verbrugge, K.
	Filing Date: July 15, 2003	Art Unit: 2188

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	A06	GHARACHORLOO, K., et al., "Memory Consistency and Event Ordering in Scalable Shared-Memory Multiprocessors," *Proceedings of the 17th International Symposium on Computer Architecture*, pages 15-26, May 1990.	
	A05	GHARACHORLOO, K., et al., "Performance Evaluation of Memory Consistency Models for Shared-Memory Multiprocessors," *Proceedings of Fourth International Conference on Architectural Support for Programming Languages and Operating Systems*, pages 245-257, 1991.	
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	A04	JOHNSON, R.E., "Extending the Scalable Coherent Interface for Large-Scale Shared-Memory Multiprocessors," *PhD Thesis, University of Wisconsin-Madison*, 1993.	
	A23	LENOSKI, D., et al., "The Directory-based Cache Coherence Protocol for the Dash Multiprocessor," *Proceedings of the 17th Int'l Symposium on Computer Architecture*, Los Alamitos, Calif., May 1990.	
	A13	LI, K., et al., "Memory Coherence in Shared Virtual Memory Systems," *ACM Transactions On Computer Systems*, 7(4):321-359, November 1989.	
	A14	LI, Q., et al., "Redundant Linked List based Cache Coherence Protocol," *World Computer Congress, IFIP Congress*, 1994.	
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	A12	MORI, S., et al., "A Distributed Shared Memory Multiprocessor: ASURA - Memory and Cache Architectures," *Supercomputing '93*, pages 740-749, Portland, Oregon, November 1993.	

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Sheet 4 of 4	First Named Inventor: Sujat Jamil	Examiner Verbrugge, K.
	Filing Date: July 15, 2003	Art Unit: 2188

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	A16	NILSSON, H., et al., "The Scalable Tree Protocol - a Cache Coherence Approach to Large-scale Multiprocessors," *Proceedings of the 4th IEEE Symposium on Parallel and Distributed Processing*, May 1992.	
	A24	NITZBERG, B., et al., "Distributed Shared Memory: A Survey of Issues and Algorithms," *IEEE Computer*, pages 52-60, August 1991.	
	A02	PAPAMARCOS, M., et al., "A Low-Overhead Coherence Solution for Multiprocessors with Private Cache Memories," *Proc. 11th ISCA*, 1984, pp. 348-354.	
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	A07	SCHEURICH, C., et al., "Correct Memory Operation of Cache-Based Multiprocessors," *Proceedings 14th Annual International Symposium on Computer Architecture*, pages 234-243, Pittsburgh, PA, June 1987.	
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	A26	THAPAR, M., et al., "Stanford Distributed Directory Protocol.," *IEEE Computer*, pages 78-80, June 1990.	
	C01	Patent Act 1977: Examination Report under section 18(3), Application No: GB0309110.5 (International App. No. PCT/US01/30359), July 7, 2004	

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Form PTO-1449 (Modified)	Atty Docket No.: 042390.P8931	Serial No.: 09/677,122
List of Patents and Publications Statement (Use several sheets if necessary) Page 1 of 2		Applicant: Sujat Jamil, et al.
		Filing Date: 09/29/2000

REFERENCE DESIGNATION — **U.S. PATENT DOCUMENTS**

Examiner Initials		Document No.		Class	Sub-Class	Filing date if appropriate
	AA					
	AB					
	AC					
	AD					
	AE					
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	AG					
	AH					
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No.		Document No.	Date	Country	Class	Sub-Class	Trans-lation
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	AR						
	AS						
	AT						
	AU						

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KV	A01	Lilja, D. J.. Cache Coherence in Large-Scale Shared-Memory Multiprocessors: Issues and Comparisons, ACM Computing Surveys, 25(3), September 1993
KV	A02	M. Papamarcos and J. Patel, "A Low-Overhead Coherence Solution for Multiprocessors with Private Cache Memories," Proc. 11th ISCA, 1984 pp. 348-354.
KV	A03	IEEE Std 1596-1992. *Scalable Coherent Interface*. Piscataway, NJ.
KV	A04	R.E. Johnson. *Extending the Scalable Coherent Interface for Large-Scale Shared-Memory Multiprocessors*. PhD thesis, University of Wisconsin-Madison, 1993.
KV	A05	Kourosh Gharachorloo, Anoop Gupta, and John Hennessy. Performance Evaluation of Memory Consistency Models for Shared-Memory Multiprocessors. In *Proceedings of Fourth International Conference on Architectural Support for Programming Languages and Operating Systems*, pages 245-257, 1991.
KV	A06	Kourosh Gharachorloo, Daniel Lenoski, James Laudon, Phillip Gibbons, Anoop Gupta, and John Hennessy. Memory Consistency and Event Ordering in Scalable Shared-Memory Multiprocessors. In *Proceedings of the 17th International Symposium on Computer Architecture*, pages 15-26, May 1990.
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KW	A12	S. Mori, H. Saito, M. Goshima, et al. A distributed shared memory multiprocessor: ASURA - memory and cache architectures -. In *Supercomputing '93*, pages 740-749, Portland, Oregon, November 1993.
KW	A13	K. Li and P. Hudak. Memory coherence in shared virtual memory systems. *ACM Transactions in Computer Systems*, 7(4):321-359, November 1989. RECE
KW	A14	Q. Li and S. Vlaovic. Redundant linked list based cache coherence protocol. In *World Computer Congress, IFIP Congress*, 1994. JAN 0
KW	A15	John M. Mellor-Crummey and Michael L. Scott. Algorithms for scalable synchronization on shared-memory multiprocessors. *ACM Trans. on Computer Systems*, 9(1), Feb 1991. Group
KW	A16	H. Nilsson and P. Stenstrom. The scalable tree protocol - a cache coherence approach to large-scale multiprocessors. In *Proceedings of the 4th IEEE Symposium on Parallel and Distributed Processing*, May 1992.
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KW	A18	Craig Anderson and Jean-Loup Baer. Design and Evaluation of a Subblock Cache Coherence Protocol for Bus-Based Multiprocessors. University of Washington, 1994, 94-05-02
KW	A19	Anderson, C. and J.-L. Baer. A Multi-Level Hierarchical Cache Coherence Protocol for Multiprocessors. University of Washington",1992, 92-10-04
KW	A20	D. Chaiken, J. Kubiatowicz, and A. Agarwal. LimitLESS directories: A scalable cache coherence scheme. In *Proc. of the Fourth Int'l Conf. on ASPLOS*, pages 224-234, New York, April 1991.
KW	A21	H. S. Sandhu, B. Gamsa, and S. Zhou. The shared regions approach to software cache coherence on multiprocessors. In *Proc. of the 4th ACM SIGPLAN Symp. on Principles and Practice of Parallel Programming*, May 1993.
KW	A22	S.J. Eggers and R.H. Katz. A characterization of sharing in parallel programs and its application to coherency protocol evaluation. In *Proceedings of the 15th Annual International Symposium on Computer Architecture*, May 1988.
KW	A23	D. Lenoski et al. The directory-based cache coherence protocol for the dash multiprocessor. In *Proc. 17th Int'l Symp. Computer Architecture*, Los Alamitos, Calif., May 1990.
KW	A24	Bill Nitzberg and Virginia Lo. Distributed shared memory: A survey of issues and algorithms. *IEEE Computer*, pages 52-60, August 1991.
KW	A25	M. Stumm and S. Zhou. Algorithms implementing distributed shared memory. *Computer*, 23(5):54-64, May 1990.
KW	A26	M. Thapar and B. Delagi. Stanford distributed directory protocol. *IEEE Computer*, pages 78-80, June 1990.
KW	A27	Shreekant Thakkar, Michel Dubios, Anthony T. Laundrie, and Gurindar S. Sohi. Scalable Shared-Memory Multiprocessor Architectures. IEEE Computer, 23(6), June 1990.

Examiner Kevin Verbrugge	Date Considered 12/20/02

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	09/677,122
Filing Date	September 29, 2000
First Named Inventor	Sujat Jamil
Art Unit	~~2185~~ 2153
Examiner Name	Kevin Verbrugge
Attorney Docket Number	42390P8931

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.¹	Document Number Number - Kind Code² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
KV		US-5,680,576	10-21-1997	Laudon	
		US-			
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KV		EP 0 397 994 A2	11-22-1990	International Business Machines Corporation		

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Sheet 2 of 2

Complete if Known	
Application Number	09/677,122
Filing Date	September 29, 2000
First Named Inventor	Sujat Jamil
Art Unit	~~2185~~ 2188
Examiner Name	Kevin Verbrugge
Attorney Docket Number	42390P8931

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KV	B02	PONG, F., et al., "Correctness of a Directory-Based Cache Coherence Protocol: Early Experience." IEEE, 1993, pgs. 37-44.	
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